Notice of Allowability	Application No.	Applicant(s)	
	10/623,276	NISHIMAKI, TATSUO	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *18 July 2003 filing*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *18 July 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date sep2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

SHAWN RILEY
PRIMARY EXAMINER

DETAILED ACTION

Reasons for Allowance

1. The following is an examiner's statement of reasons for allowance: No prior art uncovered anticipates or renders obvious applicant(s) claimed power source circuit including means for producing a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the CMOS inversion circuit, controlling the PWM signal supplied to the gate of the N-channel transistor among PWM signals supplied to the CMOS inversion circuit by the detection signal from the detection circuit, and turning "off" an "on" state of the N-channel transistor.

Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed power source circuit including a current feedback circuit producing a current feedback signal according to a magnitude of a load current based on the detection signal showing the zero point position; means for obtaining an error signal by comparing the current feedback signal with a predetermined reference voltage value; and means for producing a PWM signal of which a pulse width is controlled by the error signal, and supplying the PWM signal to each gate of the CMOS inversion circuit.

Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed power source circuit including means for obtaining an error signal by comparing the current feedback signal with a predetermined reference voltage value; and means for producing a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the

CMOS inversion circuit, at the same time, controlling the PWM signal supplied to the gate of the N-channel transistor among PWM signals supplied to the CMOS inversion circuit by the first detection signal from the detection circuit, and turning "off" an "on" state of the N-channel transistor.

Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed power source circuit including a detection circuit outputting a detection signal showing a state where an intermediate node potential at a connection point of the high side transistor and the low side transistor surpasses the reference potential after undershooting to a level lower than the reference potential when the low side transistor is turned "on" during the "off" period of the high side transistor; and means for controlling the PWM signal supplied to the gate of the low side transistor among PWM signals supplied to the DC-DC conversion circuit by the detection signal from the detection circuit, and turning "off" an "on" state of the low side transistor.

2.

Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed power source circuit including a detection circuit outputting a detection signal showing a state where an intermediate node potential at a connection point of the high side transistor and the low side transistor surpasses the reference potential after undershooting to a level lower than the reference potential when the low side transistor is turned "on" during the "off" period of the high side transistor; means for obtaining an error signal by comparing the output from the DC-DC conversion circuit with a predetermined reference voltage value; and means for producing a

PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the DC-DC conversion circuit, controlling the PWM signal supplied to the gate of the low side transistor among PWM signals supplied to the DC-DC conversion circuit by the detection signal from the detection circuit, and turning "off" an "on" state of the low side transistor.

3. Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed power source circuit including a detection circuit detecting a zero point position when a potential at a connection point of the high side transistor and the low side transistor returns to the reference potential after undershooting to a level lower than the reference potential, and outputting a detection signal that shows at least the zero point position when the low side transistor is turned "on" during the "off" period of the high side transistor; a current feedback circuit producing a current feedback signal according to a magnitude of a load current based on the detection signal showing the zero point position; means for obtaining an error signal by comparing the current feedback signal with a predetermined reference voltage value; and means for producing a PWM signal of which a pulse width is controlled by the error signal, and supplying the PWM signal to each gate of the DC-DC conversion circuit.

Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed power source circuit including the transistors being alternately turned "on" or "off" by a PWM signal input to a gate of each transistor with an "on" period of the transistors being controlled, and

being capable of outputting a D.C. voltage to a load via a stabilized capacitance; a detection circuit outputting a detection signal showing a state where an intermediate node potential at a connection point of the P-channel transistor and the N-channel transistor surpasses the reference potential after undershooting to a level lower than the reference potential when the N-channel transistor is turned "on" during the "off" period of the P-channel transistor; an error amplifier that obtains an error signal by comparing an output from the CMOS inversion circuit with a predetermined reference voltage value; and a PWM circuit and output driver that produce a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the CMOS inversion circuit, controlling the PWM signal supplied to the gate of the N-channel transistor among PWM signals supplied to the CMOS inversion circuit by the detection signal from the detection circuit, and turning "off" an "on" state of the N-channel transistor.

Further, no prior art uncovered anticipates or renders obvious applicant(s) claimed power source circuit including a detection circuit outputting a first detection signal showing a state where a potential at a connection point of the high side transistor and the low side transistor surpasses the reference potential after undershooting to a level lower than the reference potential, at the same time, detecting a zero point position when the potential at the connection point returns to the reference potential after undershooting to the level lower than the reference potential, and outputting a second detection signal that shows at least the zero point position when the low side transistor is turned "on" during the "off" period of the high side transistor; a current feedback circuit producing a current feedback signal according to a magnitude of a load

current based on the second detection signal showing the zero point position; means for obtaining an error signal by comparing the current feedback signal with a predetermined reference voltage value; and means for producing a PWM signal of which a pulse width is controlled by the error signal, supplying the PWM signal to each gate of the DC-DC conversion circuit, at the same time, controlling the PWM signal supplied to the gate of the low side transistor among the PWM signals supplied to the DC-DC conversion circuit by the first detection signal from the detection circuit, and turning "off" an "on" state of the low side transistor.

Allowable Subject Matter

1. Claims 1-20 are allowable over the prior art of record.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

November 04

Shawn Riley
Primary Examiner